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The electrical and interface properties of metal-ferroelectric (lanthanum substituted bismuth titanate: BLT)-insulator-semiconductor (MFIS) structures with various insulators

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Abstract We have investigated metal-ferroelectric-insulator semiconductor (MFIS) structures with lanthanum substituted bismuth titanate (BLT) as a ferroelectric layer and lanthanum oxide (LO) or zirconium silicate (ZSO) as an insulating buffer layer between BLT and Si substrate. The morphology of BLT films deposited on LO or ZSO oxide was not changed due to the good thermal stability of LO and ZSO films. But an interface reaction between BLT and buffer layer started at high annealing temperature (750 °C), which was confirmed by transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS). The maximum memory window was 3.59 V at a sweep voltage of 7 V with the LO film annealed at 650 °C and a thickness of 5 nm. With BLT/LO annealed at 750 °C, the window was decreased due to the reaction between the BLT film and LO. The memory window was about 1 V lower with a ZSO film because ZSO film has a lower dielectric constant than LO film. The MFIS structure annealed at 750 °C had a lower leakage current density because the electrical properties of the buffer layer (La oxide or Zr silicate) were improved by the thermal process.

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Introduction

Considerable attention has been directed towards ferroelectric materials since nonvolatile memory devices using ferroelectric storage capacitors were proposed in the latter half of the 1980s. Also ferroelectric gate field effect transistor (FET)-type memory is recognized to be excellent due to its nondestructive readout (NDRO) capability [1] and compliance with the scaling rule compared to the destructive readout (DRO) storage capacitor-type.

The ferroelectric random access memory (FRAM) with NDRO operation employs a metal gate FET with ferroelectric gate dielectric on top of semiconductor silicon [2]. To realize a practical ferroelectric FET, ferroelectric films should satisfy the following criteria: large remanent polarization (Pr), low coercive field, low dielectric loss, high resistivity, and stable interface with Si. But metal-ferroelectric-semiconductor (MFS) structures have serious problems because unwanted SiO_2 and the interfacial layer can be formed between the ferroelectric thin film and the substrate silicon while depositing and annealing the ferroelectric thin film on the semiconductor substrate [3, 4]. It becomes difficult to apply sufficient voltage to the ferroelectric film because the dielectric constant of ferroelectric films is much higher than that of SiO_2. Consequently, it needs high operating voltage to apply a large enough voltage to reverse the polarization of the ferroelectric film. To overcome these problems, inserting a buffer layer such as CeO_2 [5], Y_2O_3 [6], $SrTiO_3$ [7], Bi_2O_3 [8], SiO_2 [9], or La_2O_3 [10] has been tried. Especially, since La_2O_3 (LO) has a high dielectric constant [11] and a high band gap (5.9 eV) [12], it is expected that LO thin film will play a role as a good charge-injection barrier

as well as improving the permittivity in the metal-ferroelectric-insulator semiconductor (MFIS) structure. Also zirconium silicate (ZSO) has recently attracted increasing interests due to its outstanding properties as a gate dielectric. It is thermally stable with Si and a good barrier against oxygen diffusion [13].

Several ferroelectric materials such as $Bi_4Ti_3O_{12}$ (BTO) [14], $SrBi_2Ta_2O_9$ (SBT) [6], $BaTiO_3$ [15], $Pb_5Ge_3O_{11}$ [16], and $YMnO_3$ [17] have been studied for MFIS structure. Among the ferroelectric materials, Pb-based perovskite thin films suffer from reliability problems such as fatigue and imprint in polarization-electric field (P-E) hysteresis loop. Therefore, bismuth layer structured ferroelectrics such as SBT and $Bi_{4-x}La_xTi_3O_{12}$ (BLT) were widely studied owing to the superior ferroelectric properties such as fatigue-free nature, little tendency of imprint, low switching voltage and long retention [18, 19]. Especially, lanthanum-modified BTO, i.e., BLT, has been suggested as a candidate material for FRAM devices [20]. BLT was suggested for a capacitor structure (DRO type) with low processing temperatures and it can also be applied to a MFIS structure (NDRO type). Preparation of BLT film on a SiO_2 buffer layer by metal organic decomposition (MOD) method was reported [21] but the interface composition and morphology were not studied. The interface properties between the ferroelectric gate dielectric, the buffer layer and the silicon substrate are very important, since the field effect in MFSFET is sensitively influenced by the interface between the Si substrate, the buffer layer and the ferroelectric thin film.

In this study, we report the deposition of BLT films on a buffer layer on p-type Si(100) substrate. The films were deposited by direct liquid injection-metal organic chemical vapor deposition (DLI-MOCVD) method and atomic layer deposition. We have investigated characteristics of the crystal structure, the morphology of the film, the interface reaction between BLT film, buffer layer, and Si substrate. The electrical properties of Au/BLT/buffer layer/Si structure with LO or ZSO as an insulating buffer layer for the MFIS-FET were also studied as a function of the thickness of a buffer layer and annealing temperature.

Experimental

We have selected $Bi(Ph)_3$ (Ph = phenyl), $La(tmhd)_3$-PMDT (tmhd = 2,2,6,6-tetramethyl-3,5-heptanedionate; PMDT = pentamethyldiethylenetriamine), and $Ti(dmae)_4$ (dimethylamino-ethoxide) as a precursor for BLT thin films and a single-mixture solution of Bi, La and Ti precursors was prepared in *n*-butylacetate to be used in DLI-MOCVD experiment. A precise amount of the solution was introduced into the flash evaporator with a syringe pump. Vaporizer temperature and the feed line after vaporizer were held at 240 °C to prevent condensation and Ar was used as a carrier gas. The reactor pressure was fixed at 1.5 Torr by using a throttle valve between the pump and the reaction chamber. The concentration of Bi, La, and Ti precursor in the cocktail source was 0.21 moles/l (M), 0.03 M, and 0.08 M, respectively and the injection speed was 0.1 ml/min. The stoichiometry of the BLT film was measured to be $Bi_{3.2}La_{0.8}Ti_3O_{12}$ after the deposition. Lanthanum oxide films were deposited with a solution of $La(tmhd)_3$-TETEA (TETEA: triethoxytriethyleneamine) in *n*-butylacetate. The ZSO films were grown in a cold-wall flow-type ALD reactor. Schematic diagram of the experimental setup was shown elsewhere [22, 23]. $ZrCl_4$ (CERAC, 99.9%) and TBOS ($Si(O^nC_4H_9)_4$ = tetra-n-butylorthosilicate) were used as precursors. The source temperature (vapor pressure) of $ZrCl_4$ and TBOS were 160 °C (0.15 Torr) and 95 °C (1.1 Torr), respectively. The composition ratio (Zr/(zr + Si)) in the ZSO film was 0.3. Operating conditions of the deposition are summarized in Table 1. The wafers used were (100) oriented p-type Si with resistivity of 8 ~ 12 Ω-cm. The modified RCA method was used for the pre-deposition cleaning.

The identification of the phase and crystallinity of the grown films were investigated by X-ray diffraction (XRD) using Cu K_α radiation. The surface morphology of the film was examined using field emission-scanning electron spectroscopy (FE-SEM) and observation of the cross-sectional view of the film was carried out by field emission transmission electron microscope (FE-TEM) using JEOL JEM-2010F operating at 200 kV. To measure the thickness, ellipsometer and SEM were used. The local compositional analysis of the reaction layers was carried out with energy dispersive X-ray spectroscopy (EDS) and a nano-beam probe of 0.5 nm in diameter. For electrical characterization, MFS capacitors were fabricated with deposited ferroelectric thin films. The Au dot electrode, 6.3×10^{-4} cm^2 in area, was deposited by thermal evaporation through a metallic mask. The capacitance-voltage (C-V) characteristics were analyzed at high frequency (1 MHz) using HP 4275 multifrequency LCR meter with a sweep voltage range of –7 to + 7 V. The current-voltage (I-V) characteristics were obtained with HP 4155 semiconductor parameter analyzer to investigate the breakdown strength and the leakage current through the oxide film.

Table 1 Deposition conditions

Parameter	Condition		
	BLT	La_2O_3	Zr Silicate (ZSO)
Deposition process	DLI-MOCVD	DLI-MOCVD	ALD
Substrate temperature	400 °C	300 °C	400 °C
Precursor (concentration)	$Bi(Ph)_3$ (0.21 M) $La(tmhd)_3$-PMDT (0.03 M) $Ti(dmae)_4$ (0.08 M)	$La(tmhd)_3$-TETEA (0.05 M)	$ZrCl_4$ TBOS
Injection speed	0.1 ml/min		–
Valve on/off time (ZSO)	$ZrCl_4$:Purge:TBOS:Purge = 5 s:2 s:2 s:2 s		
Vaporizer temperature	240 °C		–
Annealing condition	O_2, 1 h		
Carrier gas (Ar)	150 sccm		20 sccm
Purge gas (Ar)	–		500 sccm
Oxidizing gas (Ar)	350 sccm		–
Deposition pressure	1.5 Torr		1 Torr
Solvent	*n*-butylacetate		–

Results and discussion

Figure 1 shows SEM micrographs of the La_2O_3 film (LO), the insulating buffer layer, with 5 nm thickness as a function of the annealing temperature. LO films were annealed in the range of 450 ~ 750 °C for 1 h. The size of the grain was independent of the annealing temperature. The grain was not detected for ZSO films because it is amorphous in our annealing temperatures [24].

Figure 2 shows SEM micrographs of the BLT film as a function of the thickness of the La oxide and the annealing temperature. All of the grain sizes in BLT on LO were similar to that on Si. The buffer layer which has thermodynamic stability did not affect the size and shape of BLT film deposited on top of it. Also the same result was obtained in the case of BLT/ZSO (Fig. 3). The average grain size is about 100 nm and it was not changed significantly with respect to the annealing temperature.

Figure 4(a) illustrates XRD pattern of the BLT film/LO (5 nm) annealed at 650 °C for 1 h. The XRD peak of BLT on LO (5 nm) was compared with that of BLT film on Si. The intensity of (117) peak was similar. However, the peak intensity of *c*-axis orientation such as (006) and (008) was smaller than that of BLT/Si. It seems that the buffer layer affects the crystallinity of the BLT film grown on it.

The BLT on Si film deposited at 400 °C was amorphous and as the annealing temperature was increased to 550 °C, the BLT thin film began to crystallize. However, the BLT (82 nm) on LO (5 nm) film was crystallized at 450 °C as shown in Fig. 4(b). It is because BLT film was deposited on the crystallized LO film. LO film becomes crystalline over 300 °C [25]. As shown in Fig. 5, The BLT on ZSO film annealed at 450 °C was amorphous and the BLT/ZSO thin film began to crystallize as the annealing temperature was increased to 550 °C. This crystallization temperature is very similar to that of BLT/Si. BLT film deposited on the amorphous ZSO film was crystallized at higher temperature. The crystallization of the BLT/LO film and BLT/ZSO was improved by increasing the annealing temperature.

Figure 6(a) shows the C-V characteristics of the Au/BLT/LO/Si structures with the film annealed at 650 °C and 750 °C. All the C-V hysteresis loops are in clockwise sweep direction and the memory window of the MFIS structure is caused by ferroelectric polarization. The memory window of the Au/BLT/LO (5 nm)/Si annealed at 650 °C was 3.59 V at 7 V sweep voltage. However, for the film annealed at 750 °C, the memory window was lower because of the reaction between the BLT film and the LO film as confirmed by the EDS analysis.

Figure 6(b) illustrates the memory window of the BLT/LO film and the BLT/ZSO film with different LO and ZSO thickness as a buffer layer. The C-V characteristic is affected by the thickness of the LO and ZSO film. When the thickness of the BLT film was fixed, the memory window showed the maximum value with LO. In the ideal MFIS structure, the applied voltage is divided into the series capacitors consisted of the BLT thin film and the buffer layer. In a MFIS structure, the electric field applied to the ferroelectric layer E_{BLT} is given by the following equation

$$E_{BLT} = \frac{\varepsilon_{Buffer}}{\varepsilon_{BLT}} E_{Buffer} \quad (1)$$

where E_{BLT} and E_{Buffer} are the effective electric field applied to the BLT film and the buffer layer. ε_{BLT} and

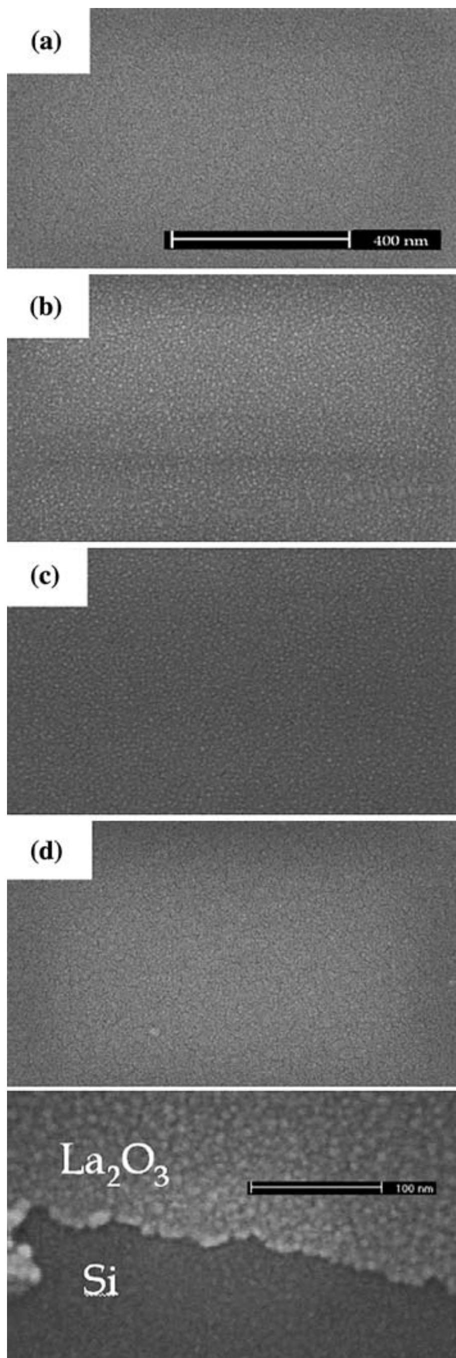

Fig. 1 SEM micrographs of the La_2O_3 film (5 nm) as a function of the annealing temperature. (**a**) 450 °C (**b**) 550 °C (**c**) 650 °C (**d**) 750 °C

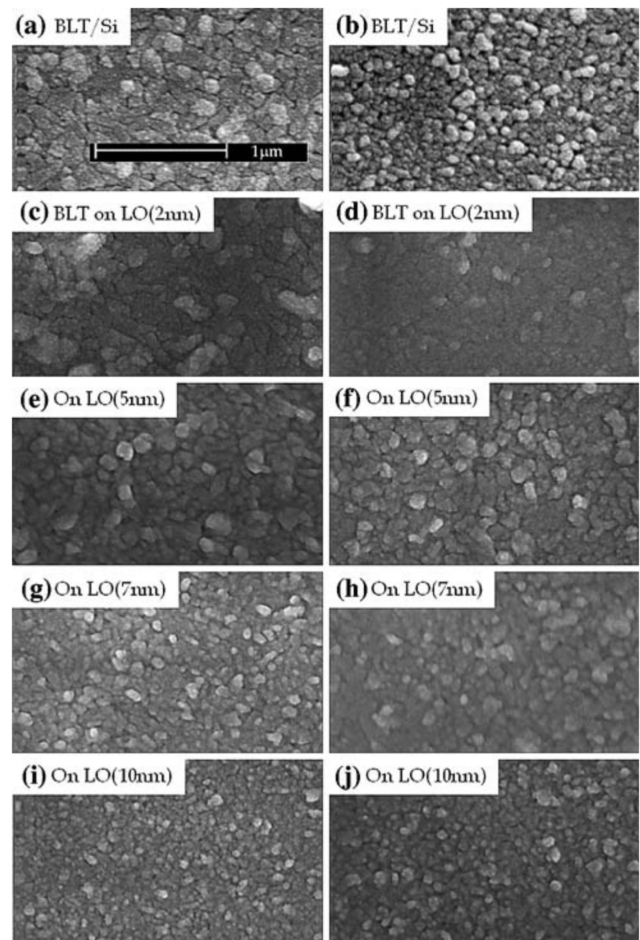

Fig. 2 SEM micrographs of the BLT film as a function of the thickness of the La oxide and the annealing temperature. (**a**), (**c**), (**e**), (**g**), and (i): 650 °C (annealing temp.), (**b**), (**d**), (**f**), (**h**), and (**j**): 750 °C

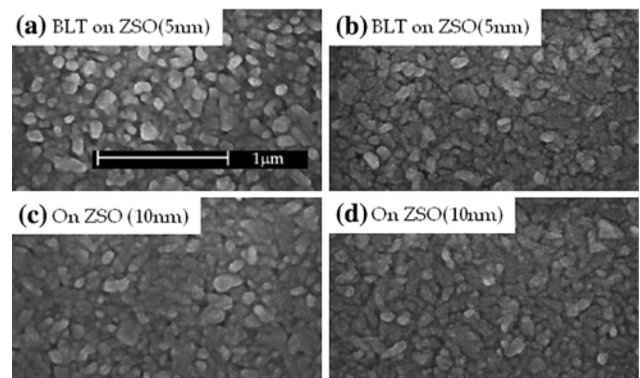

Fig. 3 SEM micrographs of the BLT film as a function of the thickness of the Zr silicate and the annealing temperature. (**a**), (**c**), (**e**), (**g**), and (i): 650 °C (annealing temp.), (**b**), (**d**), (**f**), (**h**), and (**j**): 750 °C

ε_{Buffer} are the dielectric constant of BLT and buffer layer, respectively. Since the electric field in each layer is sensitive to the thickness of the ferroelectric BLT and buffer layer, optimizing the thickness of these layers is important to obtain the required memory window. The thickness of the buffer layer is also important to minimize inter-diffusion between ferroelectric thin film and Si substrate and the charge injection. In addition to this, the applied voltage to the BLT film is determined by the thickness of the buffer

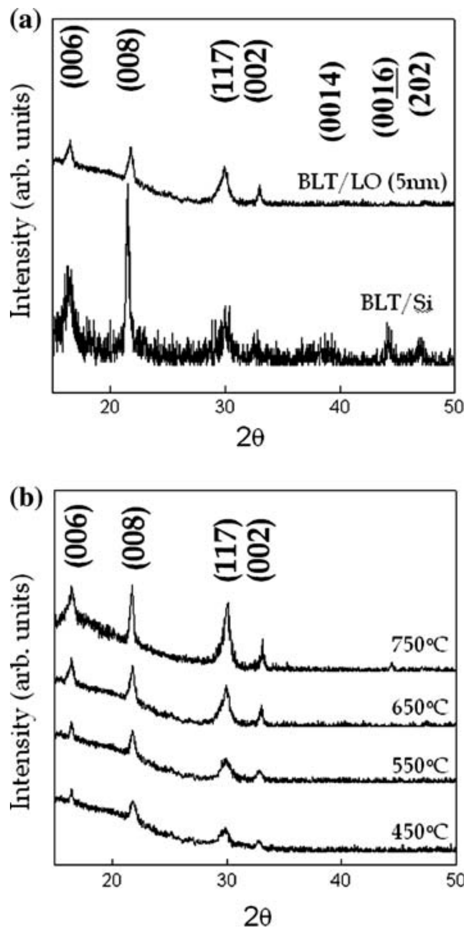

Fig. 4 (**a**) XRD pattern of the BLT (85 nm) film annealed at 650 °C on La_2O_3 (5 nm) film and on Si substrate for 1 h in O_2 ambient. (**b**) XRD pattern of the BLT (85 nm) film deposited at 400 °C on La_2O_3 (5 nm) film and annealed in the range of 450 ~ 750 °C for 1 h in O_2 ambient

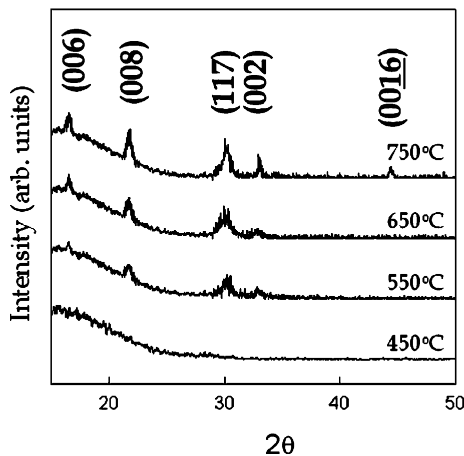

Fig. 5 XRD pattern of the BLT (85 nm) film on Zr silicate (5 nm) film annealed in the range of 450 ~ 750 °C for 1 h in O_2 ambient

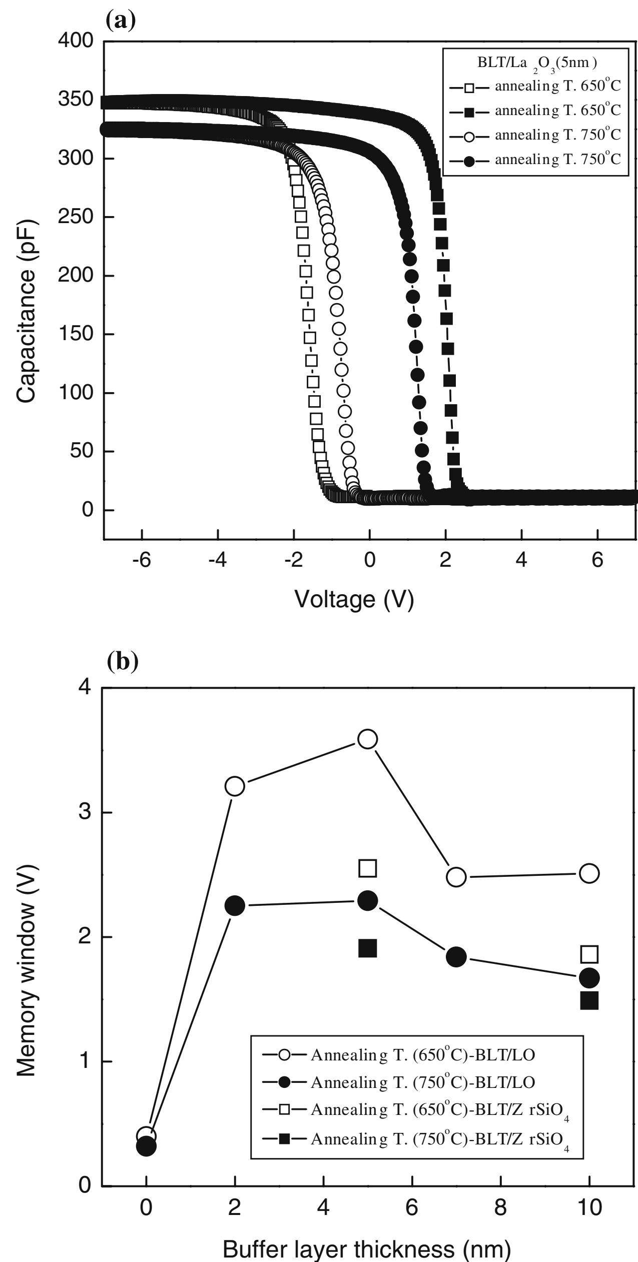

Fig. 6 (**a**) C-V characteristics of Au/BLT/LO (5 nm)/Si structures, with BLT/BO film annealed at 650 and 750 °C. (**b**) Variation in the memory window with the LO thickness and ZSO thickness

layer when the BLT film thickness is fixed. The reduction of the E_{BLT} by the decrease of E_{Buffer} results in the decrease in the memory window of the ferroelectrics. The memory window of the BLT film on 2 nm thick LO was higher than that without buffer layer. However, it was smaller than that with 5 nm thick LO, and is because of the charge injection into the BLT film by the applied voltage. The thick buffer layer was helpful to block the charge injection but

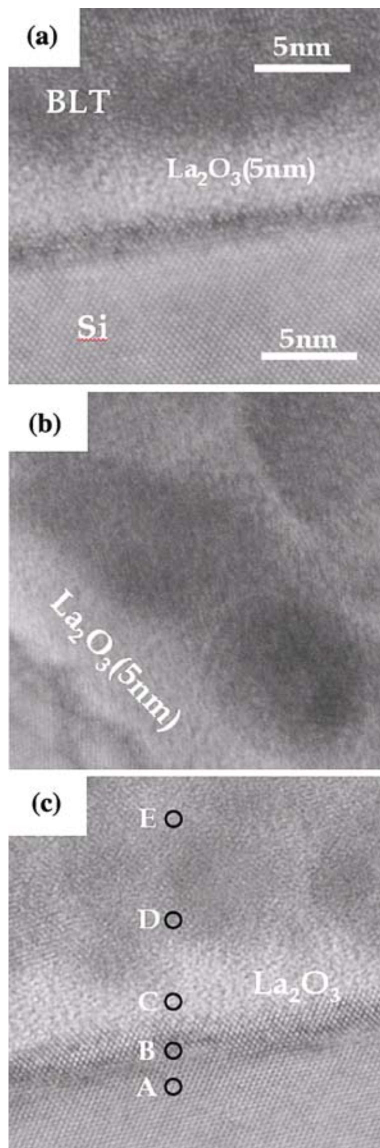

Fig. 7 Cross-sectional TEM image of the BLT film on the La oxide film (5 nm). The film was (**a**) deposited at 400 °C (**b**) annealed at 650 °C, and (**c**) at 750 °C

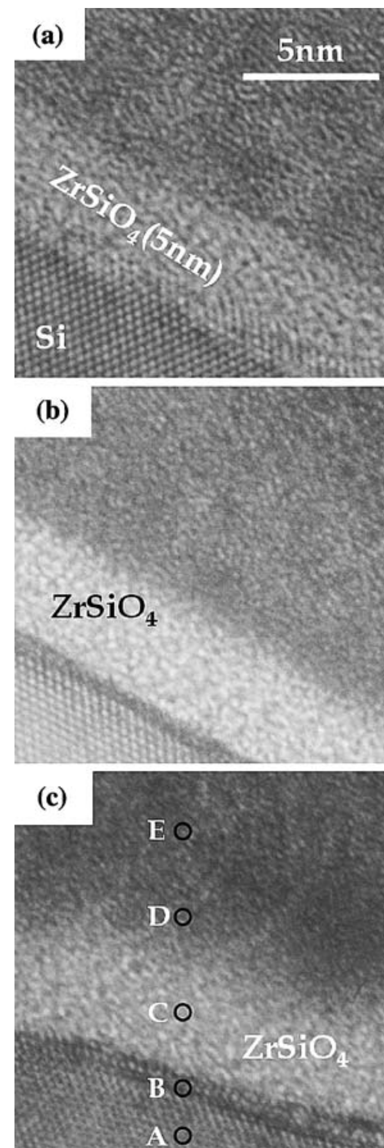

Fig. 8 Cross-sectional TEM image of the BLT film on the Zr silicate film (5 nm). The film was (**a**) deposited at 400 °C (**b**) annealed at 650 °C, and (**c**) at 750 °C

when the thickness of the LO film exceeds 5 nm (7 and 10 nm), the memory window of the MFIS structure was smaller, due to the decrease of the E_{Buffer}. With the reduction of E_{Buffer}, the E_{BLT} was decreased as shown in Eq. (1). We confirmed that the optimum thickness of the LO film was 5 nm when the BLT film was fixed at 85 nm. When the film was annealed at 750 °C, the memory window was decreased owing to the reaction between the BLT film and the LO film. When using ZSO film as a buffer layer, the memory window of BLT/ZSO (5 nm) was higher than that of BLT/ZSO (10 nm) for the same reason. The memory window was 2.55 V at the sweep voltage of 7 V with ZSO film annealed at 650 °C and with same thickness of 5 nm as the LO film. It is about 1 V lower compared with BLT/LO. This is because the ZSO film (dielectric constant (k) = 9) has a lower dielectric constant than LO film (k = 23) (Eq. (1)). The 10 nm thick LO and ZSO film were used to measure the dielectric constant. The memory window of BLT/ZSO (10 nm) film was lower than that of BLT/ZSO (5 nm) because of the decrease in the electric field which was applied to the BLT film. The memory window of BLT/LO (5 nm) annealed at 450 °C and 550 °C was 0.2 and 0.3 V, respectively.

Figures 7, 8, and 9 show a cross-sectional TEM image and the EDS quantification of the film composition plotted with respect to the location defined by open circles, respectively. The thickness of the BLT

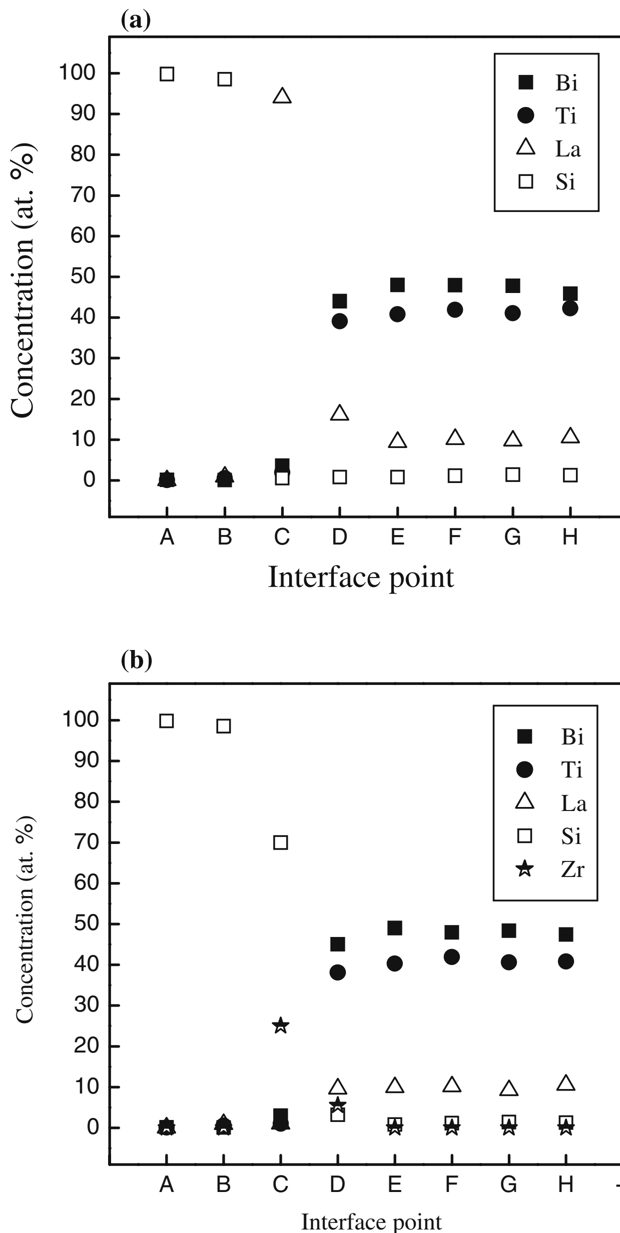

Fig. 9 Film composition at different locations measured with 0.5 nm beam-EDS. Each location was shown by open circles in Fig. 7(c) and Fig. 8(c). The BLT film of 85 nm thickness was annealed at 750 °C in O_2 ambient for 1 h. (**a**) BLT/LO film (**b**) BLT/ZSO film

film, LO layer and ZSO layer was measured by TEM analysis as shown in Fig. 7(a) and Fig. 8(a). The ZSO film deposited by ALD process had a better uniformity than the LO film deposited by DLI-MOCVD process. After annealing at 750 °C, the thickness of the buffer layer was not changed, but the interface was blurred due to the interdiffusion and interaction between BLT film and buffer layer in both cases.

Based on the morphology and composition analyzed here, the cross section could be resolved in four

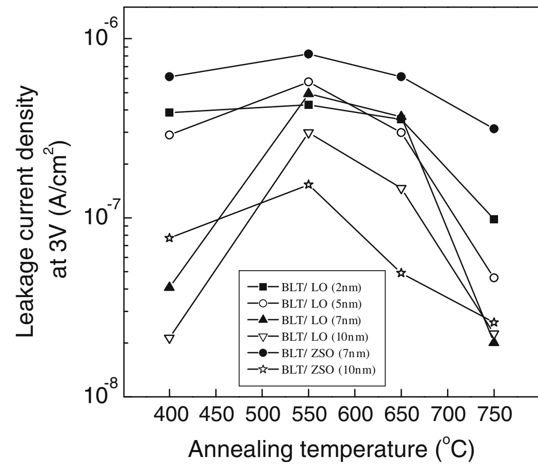

Fig. 10 I-V characteristics of the BLT film on a La oxide film and a Zr silicate film deposited at 400 °C and annealed at 550 °C, 650 °C and 750 °C

different layers: (i) Si substrate underneath the buffer layer (points A and B); (ii) buffer layer (point C); (iii) the BLT film on buffer layer (point D); (iv) the BLT film (points E, F, G, and H). The EDS point-analyzed spectra were collected in 30 s live time using 0.5 nm probe with about 10 pA/cm^2. The EDS analysis at each point was performed with a 0.5 nm diameter electron beam probe and repeated 10 times at one point within the layer. The atomic concentration of each location in the film annealed at 750 °C was plotted in Fig. 10. Bi, La, and Ti element in the substrate underneath intermediate layer were less than 1% which is in the error rage of the detection.

In case of the BLT/LO film (Fig. 9(a)), the concentration (at %) of the buffer layer formed at 400 °C was Si:Bi:La:Ti = 0.3:1.6:97.3:0.8. After the annealing (750 °C), the content of Bi, Ti, and Si in the buffer layer was increased and that of La was decreased. The composition was Si:Bi:La:Ti = 0.5:3.6:94:1.9. In point D, the content of La was higher than the bulk film due to the reaction between the BLT film and the buffer layer. However, the composition of the film at points E, F, G, and H was not changed. In case of the BLT/ZSO film, the result was similar to that of BLT/LO film. The ZSO film deposited by ALD was Si-rich Zr silicate and the composition ratio of Zr silicate film was Zr:Si = 5:14. After the annealing (750 °C), the content of Zr and Si in point D was decreased by the reaction between the BLT film and the buffer layer. By this reaction, the electrical properties became poor.

Figure 10 shows the current-voltage (I-V) characteristics of the MFIS device. All of the films annealed at 550 °C had the higher leakage current density than as-deposited film at 400 °C. It is due to the crystallization of the BLT film. When the BLT film is

crystallized, carriers can easily flow through grain boundaries and result in a larger leakage current [26]. As the thickness of the buffer layer is increased, the leakage current density is deceased and with the increase of the annealing temperature, the leakage current density was decreased because the physical and electrical properties of the buffer layer were improved by the thermal process [27].

Conclusions

We have fabricated MFIS structure with BLT as a ferroelectric thin film and LO or zirconium silicate film as an insulating buffer layer. The morphology of the BLT thin film deposited on La oxide film or Zr silicate film was independent of the morphology of the buffer layer and the annealing temperatures. The memory window of BLT/LO films was increased from 0.32 V to 3.59 V at 7 V when the thickness of La oxide films was changed from 2 to 10 nm with the 85 nm thick BLT film. The maximum memory window was 3.59 V with Au/BLT (82 nm)/LO (5 nm)/Si structure and at the annealing temperature of 650 °C. In case of BLT/Zr silicate film, the memory window was changed in the range of 1.91–2.55 V. The memory window of the BLT film deposited on Zr silicate film was lower than that on La oxide because the Zr silicate film has a lower dielectric constant. The MFIS structure annealed at 750 °C had the lowest leakage current density.

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